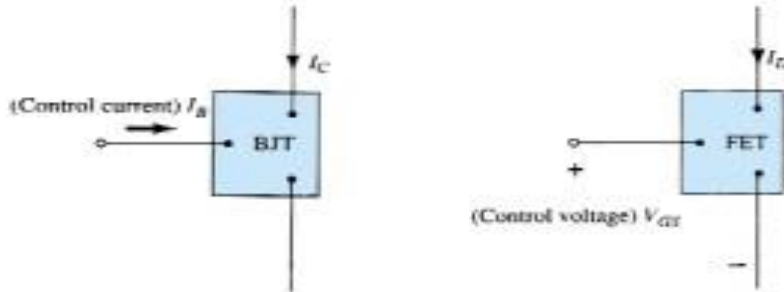


DISCLAIMER

COPYRIGHT IS NOT RESERVED BY THE CONTRIBUTOR OF THIS MATERIAL. THIS MATERIAL IS PREPARED ONLY TO HELP THE STUDENTS. VARIOUS SOURCES MAY HAVE BEEN USED/REFERRED WHILE PREPARING THIS MATERIAL. THIS DOCUMENT SHOULD NOT BE USED AS A SUBSTITUTE FOR PRESCRIBED TEXTBOOK. CONTRIBUTOR OF THIS MATERIAL IS NOT RESPONSIBLE FOR ANY LEGAL ISSUES ARISING OUT OF ANY COPYRIGHT DEMANDS AND/OR REPRINT ISSUES CONTAINED IN THIS MATERIALS. THIS MATERIAL IS NOT MEANT FOR ANY COMMERCIAL PURPOSE & ONLY MEANT FOR PERSONAL USE.

FIELD EFFECT TRANSISTOR (FET)

- The transistor is of two types:
 - i) Bipolar Junction Transistor (BJT)
 - ii) Field Effect Transistor (FET)
- In BJT, the current conduction is the function of two charge carriers, electron & hole. So it is called as *bipolar*.
- In FET, the current conduction is the function of either electron or hole. Hence it is called as *unipolar*.
- The field-effect transistor (FET) is a three-terminal device. The terminals are GATE (G), SOURCE (S) & DRAIN (D).
- The primary difference between the two types of transistors is the fact that the BJT is a *current-controlled* device while FET is a *voltage-controlled* device. In other words, the output current I_C in BJT is a direct function of input level of I_B whereas the Output current I_D in FET is controlled by input voltage.

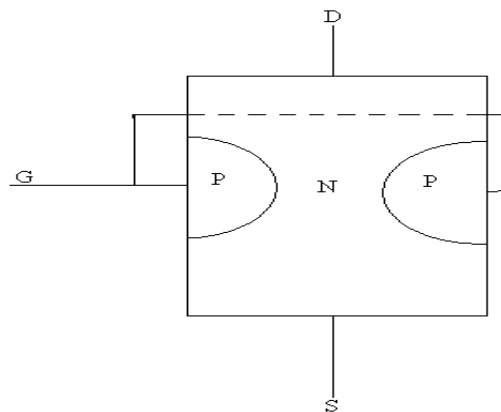


- Two types of FETs are there:
 - i) Junction Field Effect Transistor (JFET)
 - ii) Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

JUNCTION FIELD EFFECT TRANSISTOR (JFET)

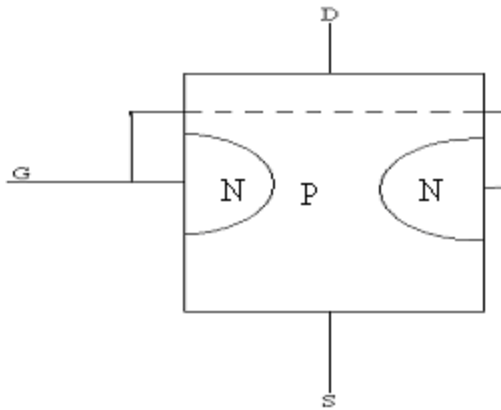
- There are two types of JFET. Such as,
 - i) n-channel JFET
 - ii) p-channel JFET

n-channel JFET



- A rectangular Slab of n-type extrinsic semiconductor in which some portions are diffused with p-type extrinsic semiconductor as shown in the figure.
- Two p-type extrinsic semiconductors are internally shorted and termed as Gate(G)
- The other two terminals are connected to n-type extrinsic semiconductors are called Drain (D) and Source (S).

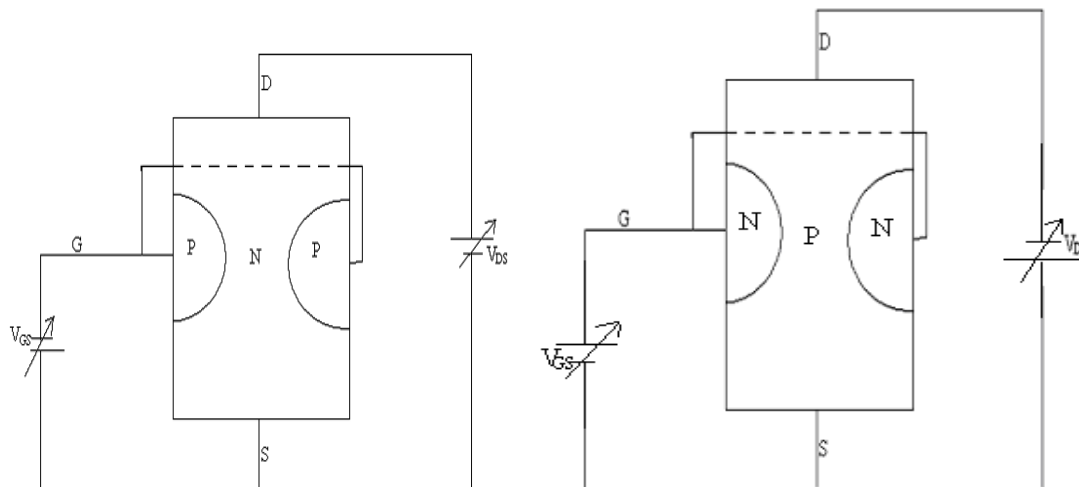
p-channel JFET



- A rectangular Slab of P-type extrinsic semiconductor in which some portions are diffused with N-type extrinsic semiconductor as shown in figure.
- Two N-type extrinsic semiconductors are internally shorted and termed as Gate (G).
- The other two terminals are connected to P-type extrinsic semiconductors are called Drain(D) and Source (S)

Polarity:

- In n-channel & p-channel JFET, the voltage between gate and source is such that the gate is always reverse biased. Hence the gate current is always zero.
- The source terminal is always connected to that end of drain voltage which provides the necessary charge carriers. For n-channel JFET, the source is connected to the negative terminal of the drain voltage supply. For p-channel JFET, the source is connected to the positive terminal of the drain voltage supply.

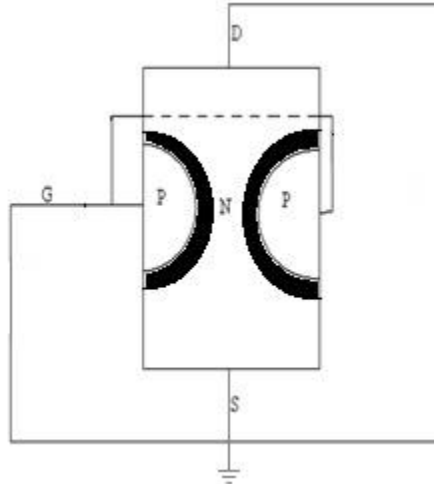


Operation:

i) n-channel JFET:

CASE-1:

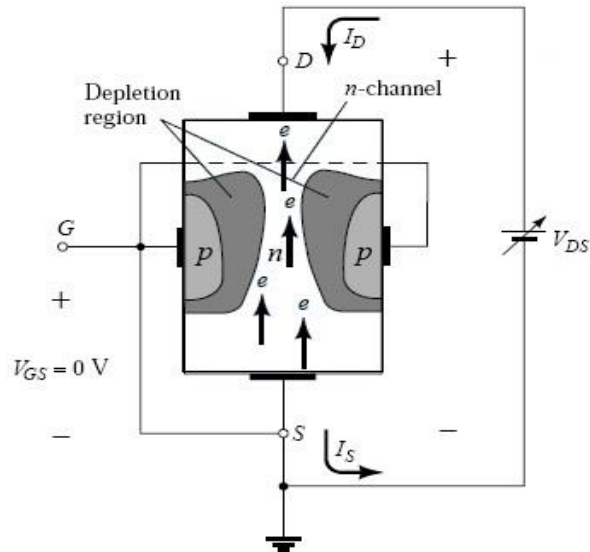
When $V_{GS} = 0$ & $V_{DS} = 0$



In this case, depletion region is formed at the two pn junction. This region has no free electron and is unable to support the current conduction. Hence the device current during this condition is zero.

CASE-2:

When $V_{GS} = 0$ & $V_{DS} > 0$ (small)

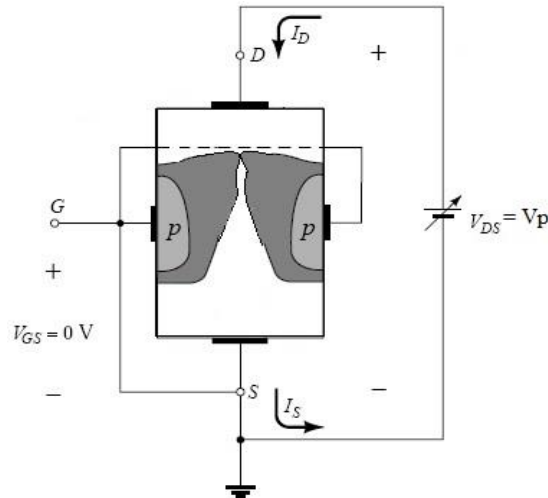


- When a small positive voltage is applied to the drain terminal with respect to the source terminal, the electrons are drawn to the drain terminal from the source terminal.
- This establishes a conventional current I_D flowing from drain terminal to source terminal.
- The path of charge flow clearly reveals that the drain and source currents are equivalent ($I_D = I_S$).
- As the voltage V_{DS} increases from 0 v to a few volts, the current also increases

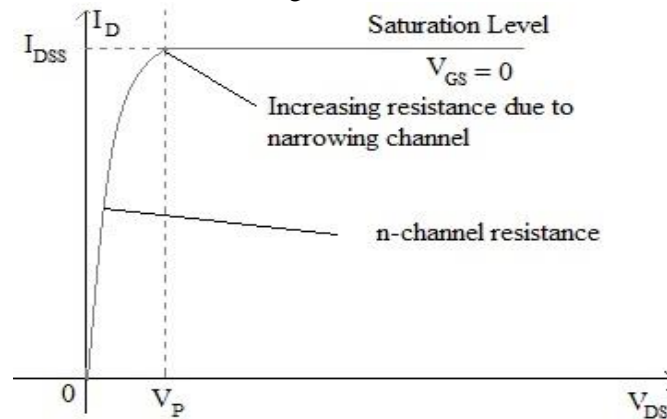
When $V_{GS} = 0$ & $V_{DS} > 0$ ($\approx V_P$)

- When the value of V_{DS} increases further, the depletion regions will widen, causing a noticeable reduction in the channel width.

- If V_{DS} is increased to a level where the two depletion regions appear to touch each other a condition referred to as *pinch-off* will occur. The level of V_{DS} that establishes this condition is referred to as the *pinch-off voltage* (V_P).



- The term *pinch-off* suggests the current I_D should pinch-off and drop to 0 A. But, I_D maintains a saturation level defined as I_{DSS} . In reality a very small channel still exists, with a current of very high density.
- The V-I characteristics of the n-channel JFET is given below:



- Mathematically,

$$V_P = V_{DS} \Big|_{V_{GS}=0 \text{ and } I_D=I_{DSS}}$$

$$\& \ I_{DSS} = I_D \Big|_{V_{GS}=0 \text{ and } V_{DS}=V_P}$$

CASE-3:

- When $V_{GS} < 0$, the pinch-off condition can be achieved with less amount of V_{DS} supply
- In this case the I_D current will be constant at low level of V_P .
- The V-I characteristic curve is shown below.

(Space for the diagram)

ii) **p-channel JFET:**

(H.W: Explain the operation of p-channel JFET with proper circuit diagrams and V-I characteristic curve)

Transfer Characteristics:

- The relation between I_D and V_{GS} is given by *Shockley's* equation as

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2$$

Here, I_{DSS} = The Saturation level of I_D

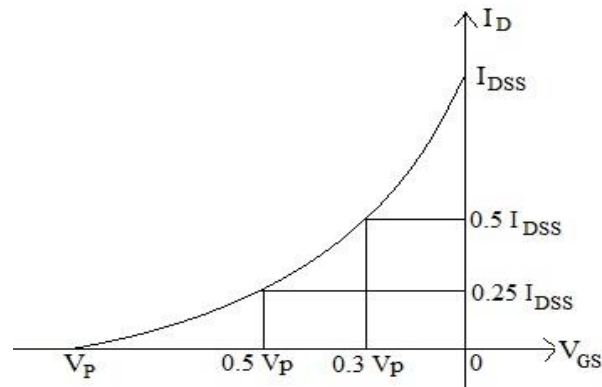
V_P = The pinch-off voltage

V_{GS} = Gate Source voltage

- It says that the drain current will tends to 0 when V_{GS} tends to V_P and I_D is maximum I_{DSS} when V_{GS} is 0V.
- From the above *Shockley's* equation, we have

V_{GS}	I_D
0	I_{DSS}
0.3 V_P	$I_{DSS}/2$
0.5 V_P	$I_{DSS}/4$
V_P	0

- Hence from the above table the transfer characteristic curve can be drawn as



PRACTICE: Sketch the transfer characteristic curve for an n-channel JFET having $I_{DSS} = 12 \text{ mA}$ & $V_P = -6 \text{ V}$.

NOTE

- For BJT, $I_C = \beta I_B$. Here since β is constant, the output current is controlled by input current. So it is called as current controlled device.
- For FET, $I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2$. Here I_{DSS} & V_P are constant, the output current is controlled by V_{GS} . So it is called as voltage controlled device.

JFET Parameters

I. AC Drain Resistance (r_d):

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D}$$

II. Transconductance (g_m):

The control that the V_{GS} have over the I_D is measured by transconductance (g_m) and is given by

$$g_m = \left. \frac{\Delta I_D}{\Delta V_{GS}} \right|_{V_{DS}=\text{CONST}}$$

III. Amplification Factor (μ):

It indicates how much more control the V_{GS} have over I_D in comparison to V_{DS} .

Mathematically,

$$\mu = \left. \frac{\Delta V_{DS}}{\Delta V_{GS}} \right|_{I_D=\text{CONST}}$$

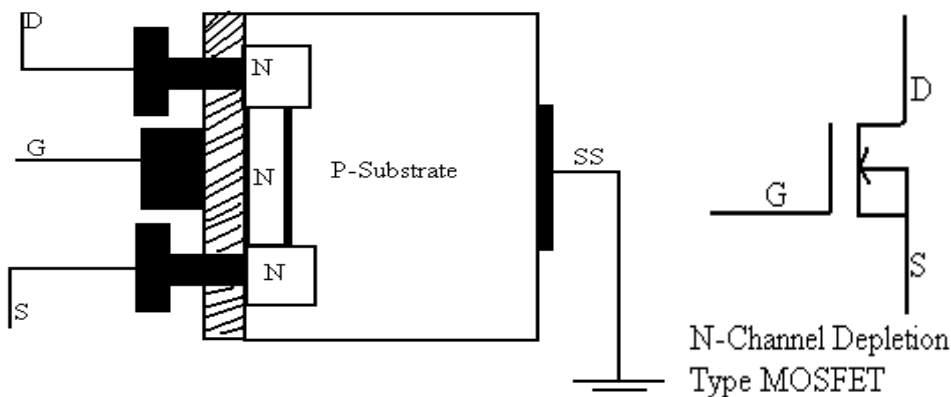
PRACTICE: Prove that $\mu = g_m \times r_d$.

MOSFET (METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR)

- It is a voltage control device, whose output current is controlled by input voltage.
- It has 4 terminals and the terminals are GATE (G), DRAIN (D), SOURCE (S) AND SUBSTRATE (Ss).
- MOSFETs are divided into *depletion type* and *enhancement type*. The terms *depletion* and *enhancement* define their basic mode of operation.
- They are further divided into n-channel and p-channel such as
 1. N-Channel Depletion Type MOSFET
 2. P-Channel Depletion Type MOSFET
 3. N-Channel Enhancement Type MOSFET
 4. P-Channel Enhancement Type MOSFET

Construction and Operation of Depletion Type MOSFET

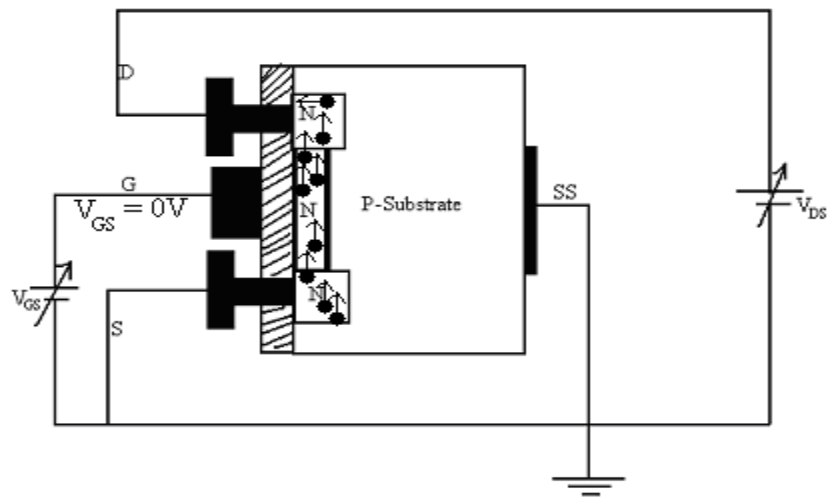
1.N-Channel



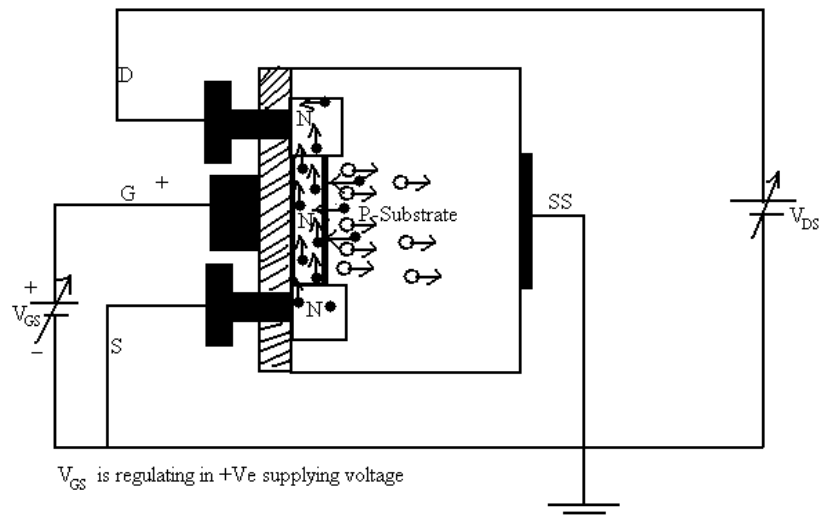
Construction:

- A slab of P-type Substrate is formed from a silicon base. It is called as substrate (Ss). The surface of the P-type substrate is then oxidized to form the insulating SiO_2 layer on it.
- Some portions of this layer are etched and two highly doped N-Type substrates are diffused into the P-type substrate.
- One of the diffused N-type substrate is called as drain (D) and the other is called as source (S). The source and drain regions are linked together and is called as channel. This channel is also N-type.
- Three Metal contacts are provided. Two out of three are inserted directly to the drain and source regions and another one is connected on the insulator and is called gate (G) terminal.
- The SiO_2 insulating layer separates the gate (G) from the channel. Due to this insulating material the device is called as insulated gate FET (IGFET).
- A ground terminal is connected to P-Type substrate by Metal contact for the reference voltage of the Device.

Operation:

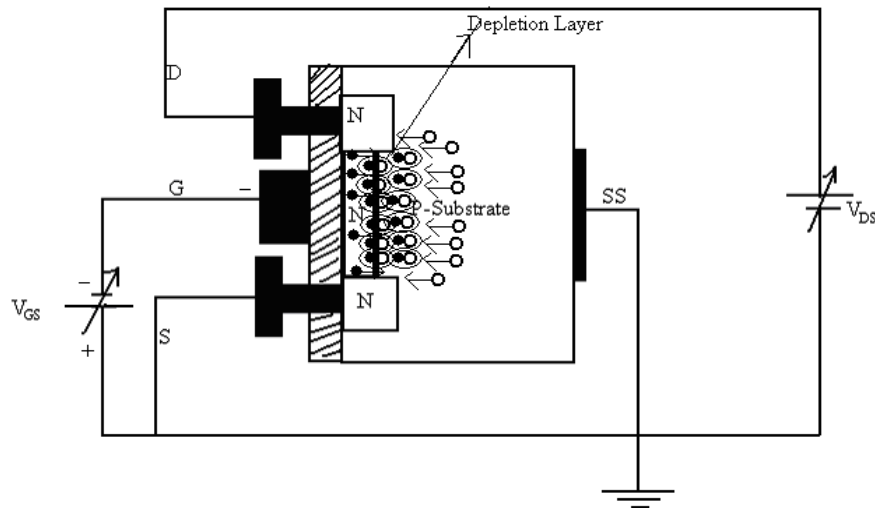


- When $V_{GS} = 0V$ and V_{DS} is regulating as the given polarity, the negative polarity of the V_{DS} repel the electrons carriers from source (S) towards the drain (D) through the N-channel.
- At the certain voltage of V_{DS} , the total electrons carriers in N-Type substrates take part in the conduction and is called Pinch-Off Voltage. Here, the current is called Drain-to-Source saturation current (I_{DSS}).



- When V_{GS} is regulating in +Ve voltage, The positive polarity at Gate will attract the electrons from the channel towards the insulator and also repel the Holes in P-substrate and attract the minority

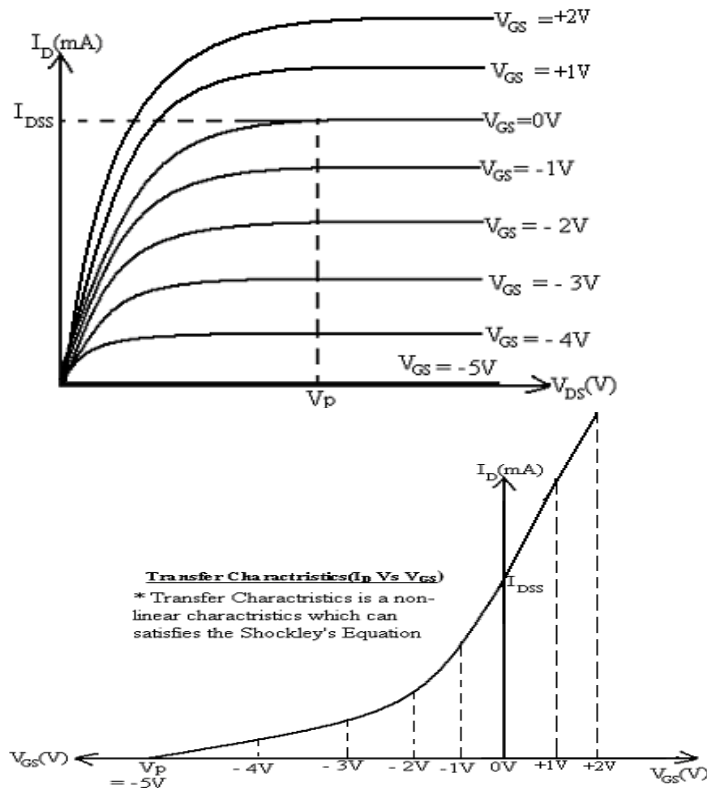
carriers(electrons) from P-substrate towards the channel/Insulator. Hence, Carriers density(Electrons) in the N-channel will increase. Therefore, The current will increase.



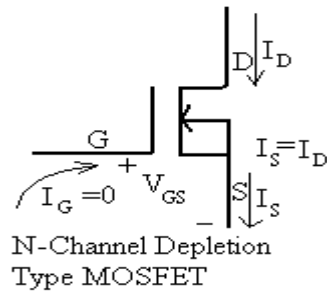
V_{GS} is regulating in $-Ve$ supply voltage

- When V_{GS} is regulating in $-Ve$ voltage, The Negative polarity at Gate will Repel the electrons from the N-channel towards the P-Type substrate and also attract the Holes from P-substrate towards the channel and Hence, a depletion layer will be formed at the junction of N-channel and P-substrate. Hence, Carriers density(Electrons) in the N-channel will decrease. Therefore, The current will decrease.
- At certain voltage of V_{GS} , no carriers in the channel take part in the conduction of current from source to drain and hence, no current flow in the channel. This voltage of V_{GS} is also called Pinch-Off voltage(V_p).

Drain Source Characteristics at different values of V_{GS} /VI characteristics of N-Channel

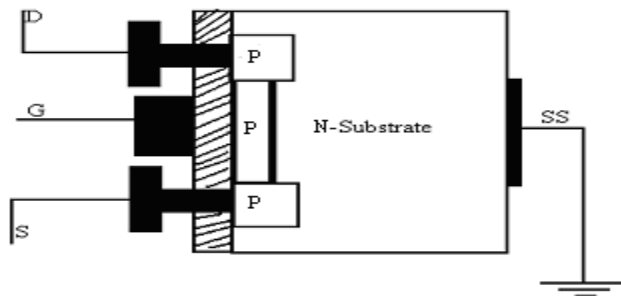


SYMBOL



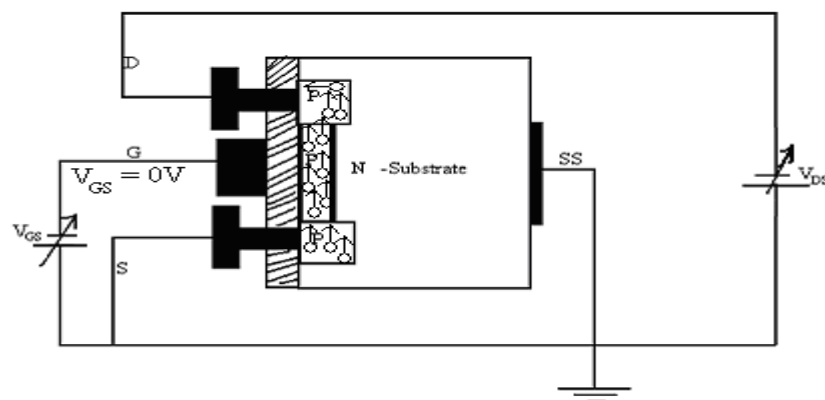
2. P-Channel

Construction

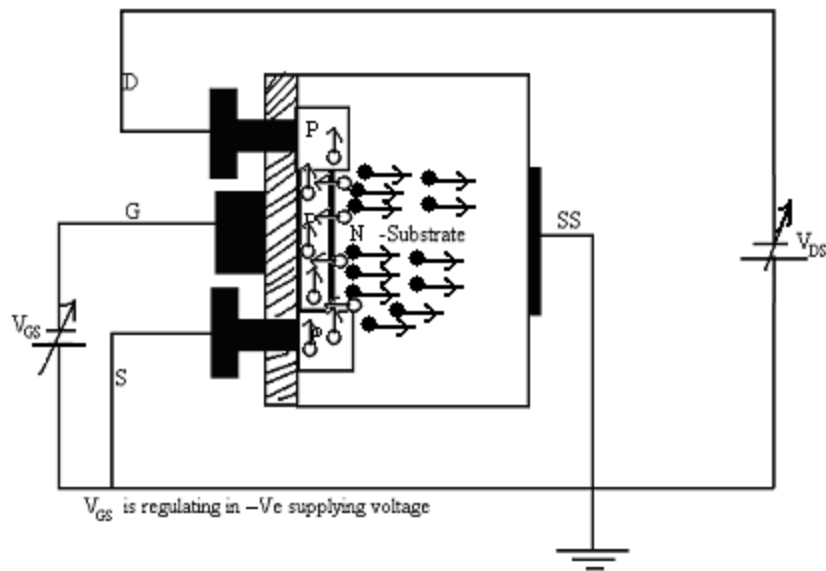


- A rectangular slab of N-Type Substrate from which some portion is etched and filled by P-Type substrate, as shown in fig.
- A channel of P-Type substrate is provided between two P-Type substrate in the rectangular slab for the conduction of current.
- An insulator (SiO_2) is provided to the P-Type substrate to separate the Gate (G) from the channel.
- Three Metal contacts are provided. Two out of three are inserted directly to P-Type substrate and the terminals are called Drain (D) and Source (S) and another one is connected on the insulator and is called Gate (G) terminal as shown in fig.
- A ground terminal is connected to N-Type substrate by Metal contact for the reference voltage of the Device.

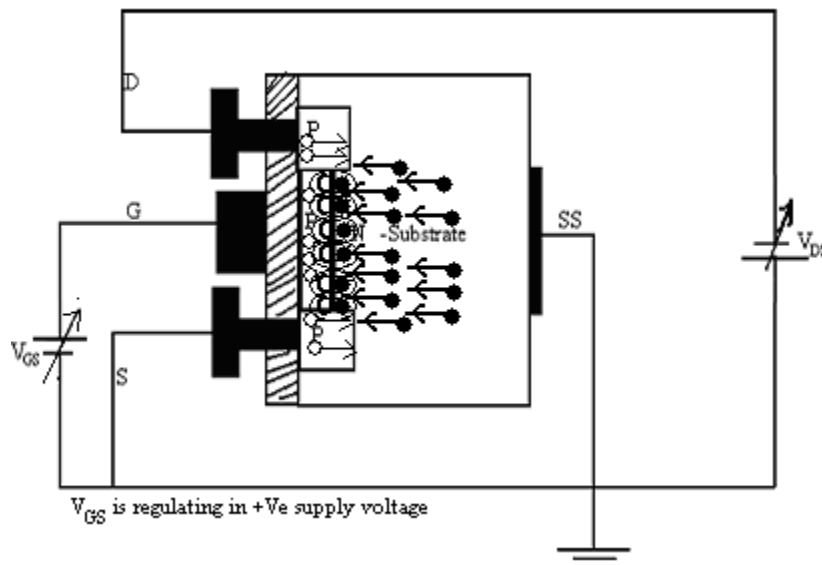
Operation:-



- When $V_{GS} = 0V$ and V_{DS} is regulating as the given polarity, the Positive polarity of the V_{DS} repel the Hole carriers from source (S) towards the drain (D) through the P-channel.
- At the certain voltage of V_{DS} , the total Hole carriers in P-Type substrates take part in the conduction and is called Pinch-Off Voltage. Here, the current is called Drain-to-Source saturation current (I_{DSS}).

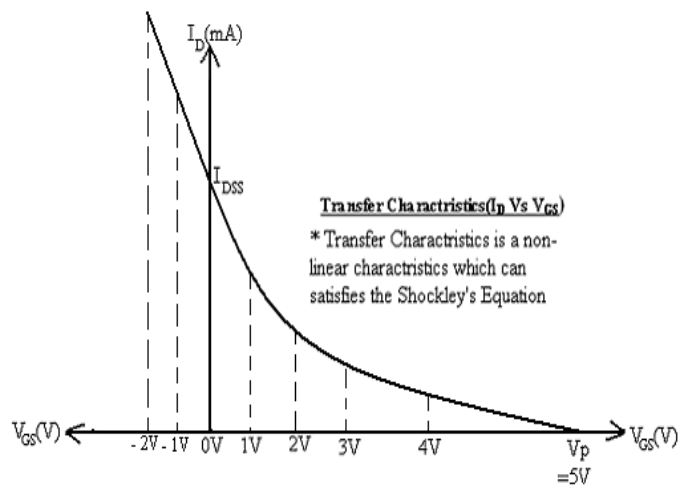
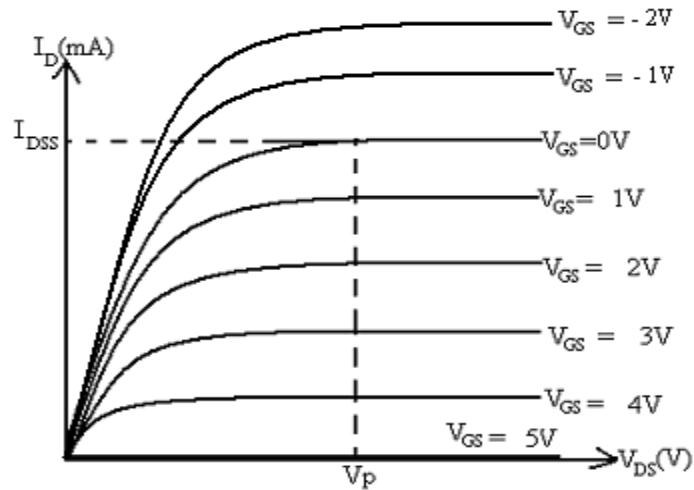


- When V_{GS} is regulating in $-Ve$ voltage, The Negative polarity at Gate will attract the Holes from the channel towards the insulator and also repel the Electrons in N-substrate and attract the minority carriers(Holes) from N-substrate towards the channel/Insulator. Hence, Carriers density(Holes) in the P-channel will increase. Therefore, The current will increase.

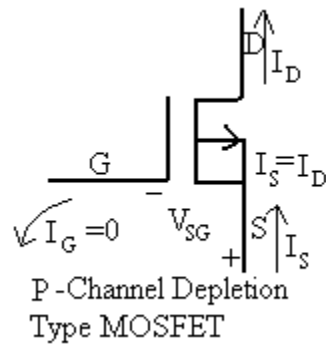
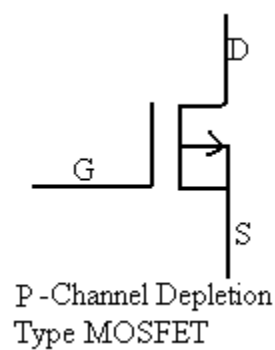


- When V_{GS} is regulating in $+Ve$ voltage, The Positive polarity at Gate will Repel the Holes from the channel towards the N-Type substrate and also attract the Electrons from N-substrate towards the channel and Hence, a depletion layer will be formed at the junction of P-channel and N-substrate. Hence, Carriers density(Holes) in the P-channel will decrease. Therefore, The current will decrease.
- At certain voltage of V_{GS} , no carriers in the channel take part in the conduction of current from source to drain and hence, no current flow in the channel. This voltage of V_{GS} is called Pinch-Off voltage(V_p).

Drain Source Characteristics at different values of V_{GS}/V_I characteristics of P-Channel



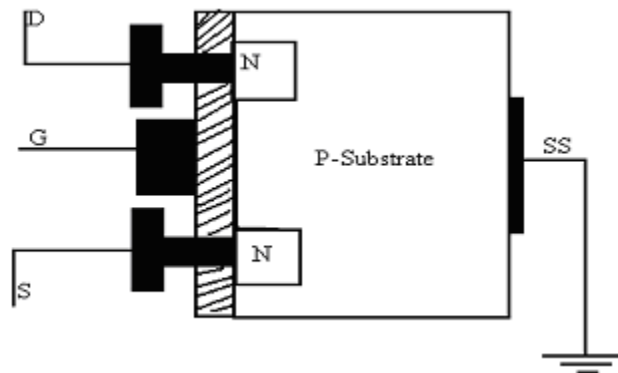
SYMBOL



Construction and Operation of Enhancement Type MOSFET

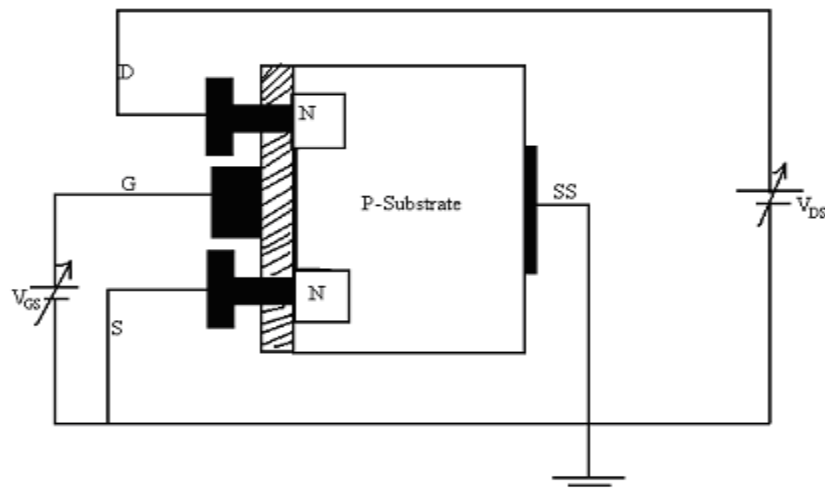
3. N-Channel

Construction

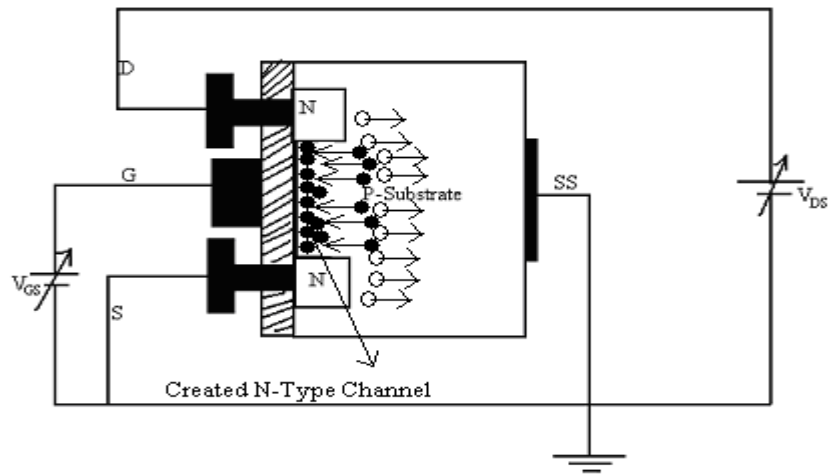


- A rectangular slab of p-Type Substrate from which some portion is etched and filled by N-Type substrate, as shown in fig.
- A channel of N-Type substrate is not provided between two N-Type substrate in the rectangular slab for the conduction of current.
- An insulator (SiO_2) is provided to the N & P-Type substrate to separate the Gate (G) from the channel.
- Three Metal contacts are provided. Two out of three are inserted directly to N-Type substrate and the terminals are called Drain (D) and Source (S) and another one is connected on the insulator and is called Gate (G) terminal as shown in fig.
- Since the channel is not present in P-substrate. Hence, a channel of N-Type will be created in between two N-Type substrate by supplying a voltage at Gate – Source terminal (V_{GS}).
- A ground terminal is connected to P-Type substrate by Metal contact for the reference voltage of the Device.

Operation:-

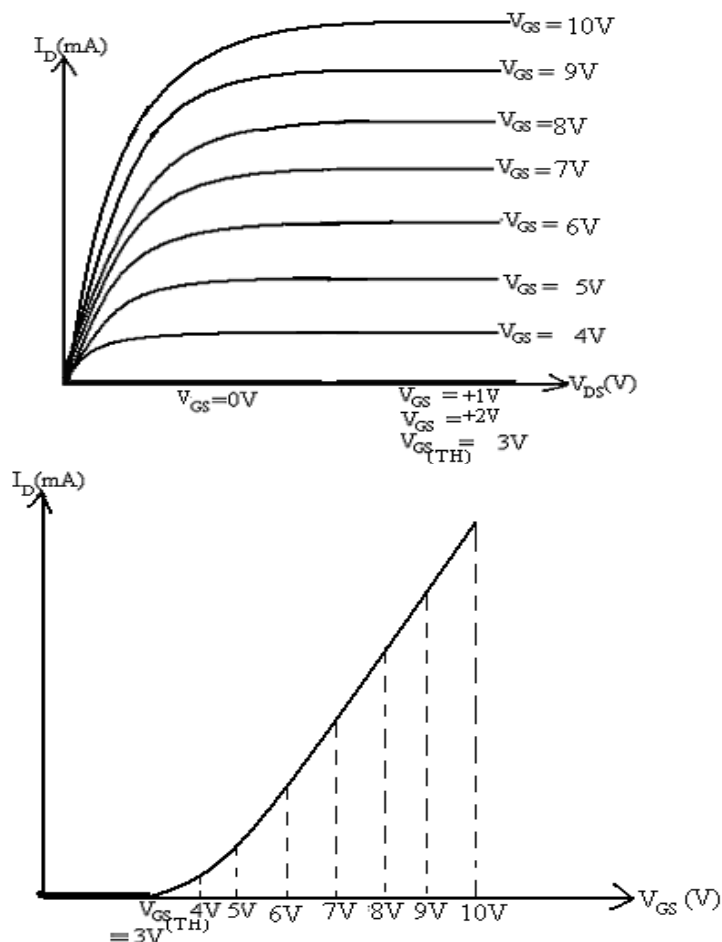


- When $V_{GS} = 0\text{V}$ and V_{DS} is regulating as the given polarity, the negative polarity of the V_{DS} repels the electrons carriers from source (S) towards the drain (D) without any N-channel. Hence no current flows from drain (D) to Source (S).
- When V_{GS} is regulating in +Ve voltage, the positive polarity at Gate will attract the electrons from the P-substrate towards the Insulator and repel the Holes in P-substrate. Hence, Carriers density (Electrons) in the N-channel will increase. Therefore, The current will increase.

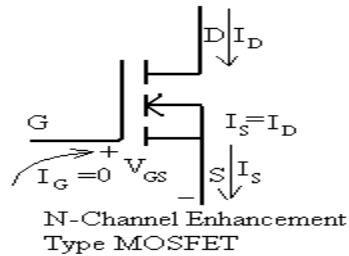
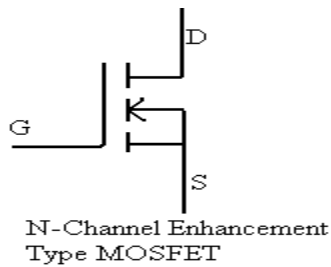


- At certain voltage of V_{GS} , Max^m minority carriers come closer towards the insulator to make an N-channel. This voltage is called Threshold voltage ($V_{GS(TH)}$). Above this voltage some extra minorities will be added in the channel to take part in the conduction of current from source to drain and hence, current flow in the channel.
- At the certain voltage of V_{GS} , there is no more minority carriers to be added in the channel. And hence, no more current will increase. This voltage is called $V_{GS(ON)}$ and the corresponding current is called $I_{D(ON)}$.

Drain Source Characteristics at different values of V_{GS} /VI characteristics of N-Channel

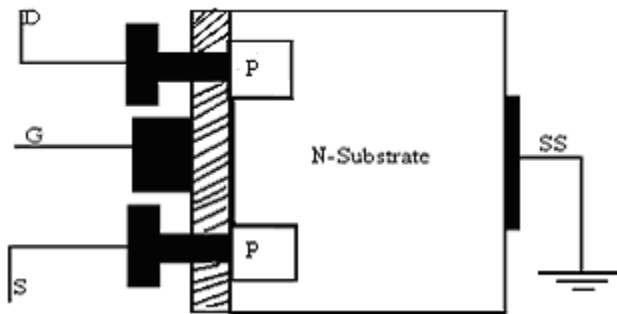


SYMBOL



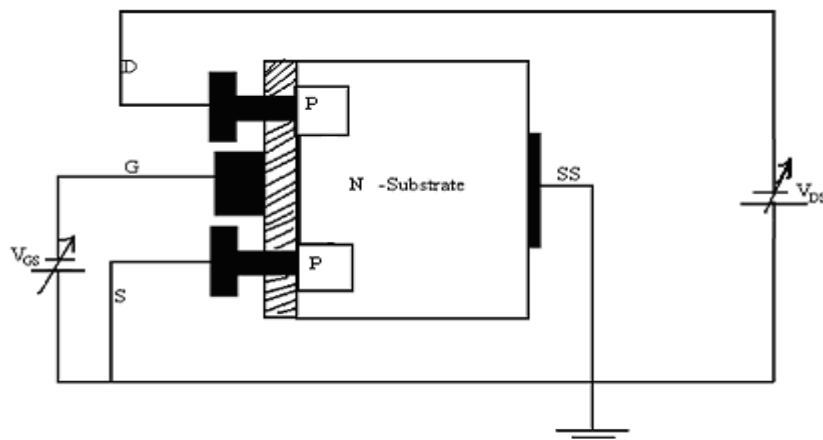
4. P-Channel

Construction

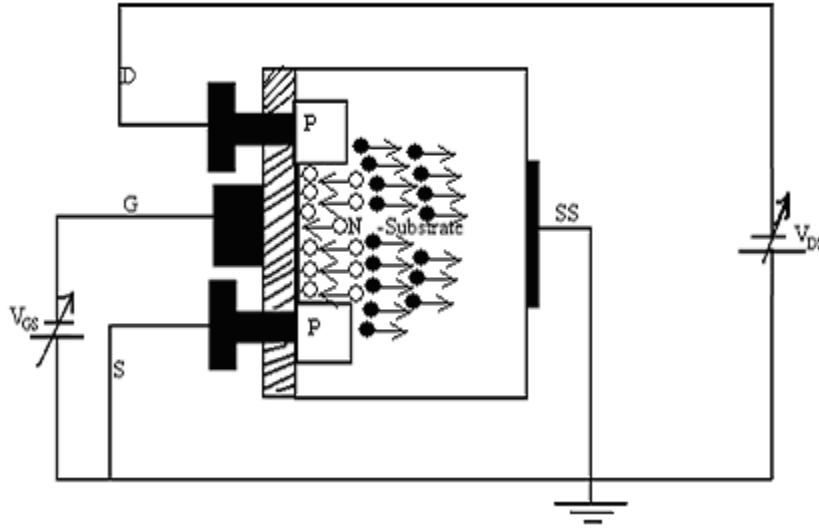


- A rectangular slab of N-Type Substrate from which some portion is etched and filled by P-Type substrate, as shown in fig.
- A channel of N-Type substrate is not provided between two N-Type substrate in the rectangular slab for the conduction of current.
- An insulator (SiO_2) is provided to the N & P-Type substrate to separate the Gate (G) from the channel.
- Three Metal contacts are provided. Two out of three are inserted directly to N-Type substrate and the terminals are called Drain (D) and Source (S) and another one is connected on the insulator and is called Gate (G) terminal as shown in fig.
- Since the channel is not present in N-substrate. Hence, a channel of P-Type will be created in between two P-Type substrate by supplying a voltage at Gate – Source terminal (V_{GS}).
- A ground terminal is connected to N-Type substrate by Metal contact for the reference voltage of the Device.

Operation:-

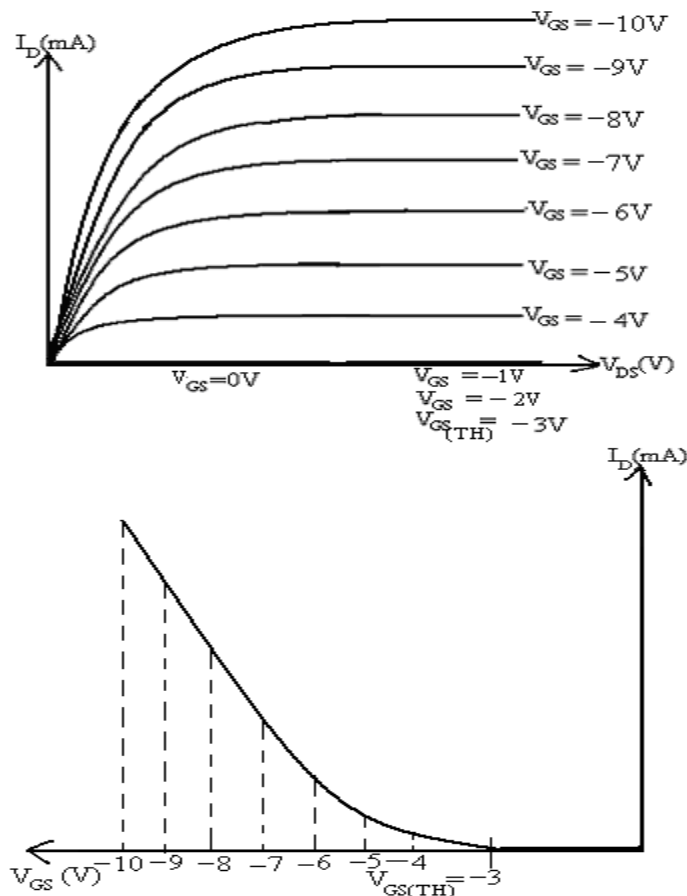


- When $V_{GS} = 0V$ and V_{DS} is regulating as the given polarity, the Positive polarity of the V_{DS} repel the Hole carriers from source(S) towards the drain(D) without any P-channel. Hence no current flow from Source(S) to Drain (D).
- When V_{GS} is regulating in -Ve voltage, The Negative polarity at Gate will attract the minority Holes from the P-substrate towards the Insulator and repel the Electrons in P-substrate. Hence, Carriers density(Holes) in the P-channel will increase. Therefore, The current will increase.

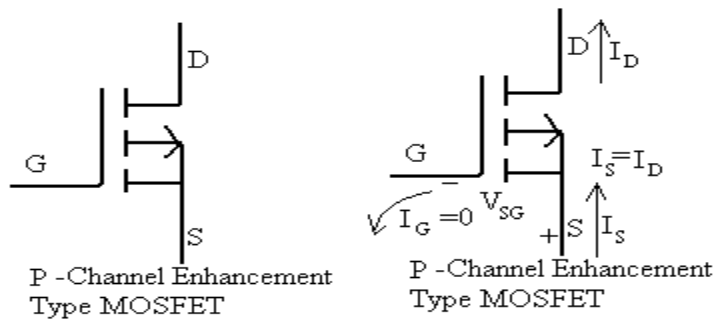


- At certain voltage of V_{GS} , Max^m minority carriers come to closer towards the insulator to make an N-channel. This voltage is called Threshold voltage($V_{GS(TH)}$). Above this voltage some extra minorities will be added in the channel to take part in the conduction of current from source to drain and hence, current flow in the channel.
- At the certain voltage of V_{GS} , there is no more minority carriers to be added in the channel. And hence, no more current will increase. This voltage is called $V_{GS(ON)}$ and the corresponding current is called $I_{D(ON)}$.

Drain Source Characteristics at different values of V_{GS} /VI characteristics of P-Channel

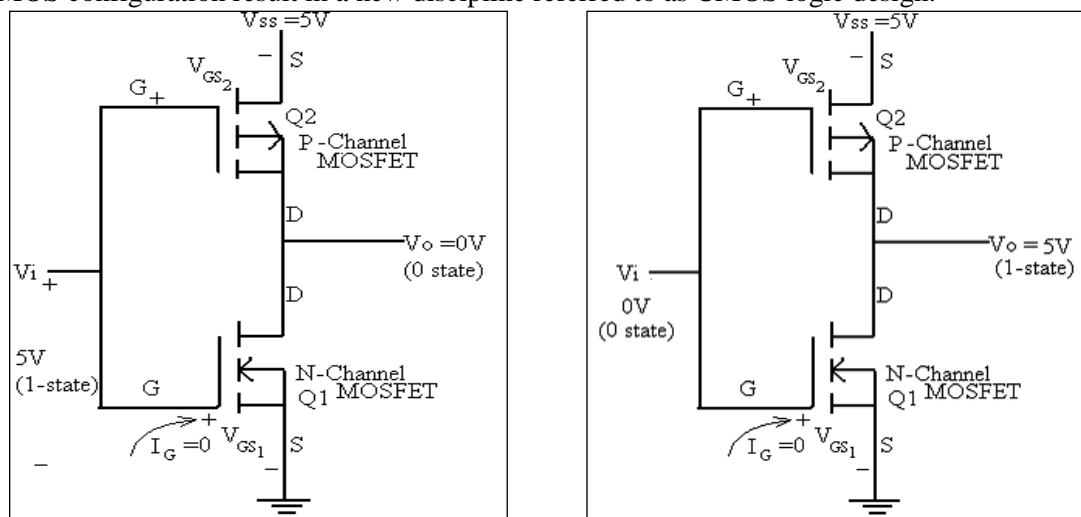


SYMBOL



CMOS

- It is a complimentary MOS having N-channel and P-channel Enhancement type MOSFET.
- It has extensive applications in computer logic design.
- Due to relatively high input impedance, fast switching speeds and lower operating power levels of CMOS configuration result in a new discipline referred to as CMOS logic design.



CMOS INVERTER

- When $V_i = 5V$ (1 state) is applied at the input terminal of the inverter, $V_{GS1} = V_i$ and hence, Q1 is 'ON', resulting in a relatively low resistance between drain and source and also, $V_{GS2} = 0V$ (because of $V_{SS} = 5V$) which is less than the Threshold Voltage ($V_{GS(TH)}$) and hence, resulting an OFF state., no current flow from source to drain in Q2. Therefore, $V_o = 0V$ (0 state).
- When $V_i = 0V$ (0 state) is applied at the input terminal of the inverter, $V_{GS1} = 0V$ and hence, Q1 is 'OFF', resulting in a relatively High resistance between drain and source and also, $V_{GS2} = 5V$ (because of $V_{SS} = 5V$ and $V_{G2} = 0V$) which is more than the Threshold Voltage ($V_{GS(TH)}$) and hence, resulting an ON state., current flow from source to drain in Q2. Therefore, $V_o = 5V$ (1 state).